

FIG. 1 is a block diagram of a communication system 10. The system 10 includes a receiver 12 and a transmitter 14. The receiver 12 includes a low noise amplifier (LEQ) 12, a demodulator (DEM) 14, a radio frequency (ROF) 16, an equalizer (EQL) 18, an automatic gain control (AGC) 20, and a detector (DET) 22. The transmitter 14 includes a modulator (MOD) 28, a radio frequency (ROF) 26, and a signal generator (SIG) 24. The receiver 12 and transmitter 14 are connected to a central processing unit (CPU) 32. The CPU 32 is connected to a data source 30. The data source 30 provides a received signal to the receiver 12 and a send signal to the transmitter 14. The receiver 12 outputs a send signal to the transmitter 14. The transmitter 14 outputs a received signal to the receiver 12.

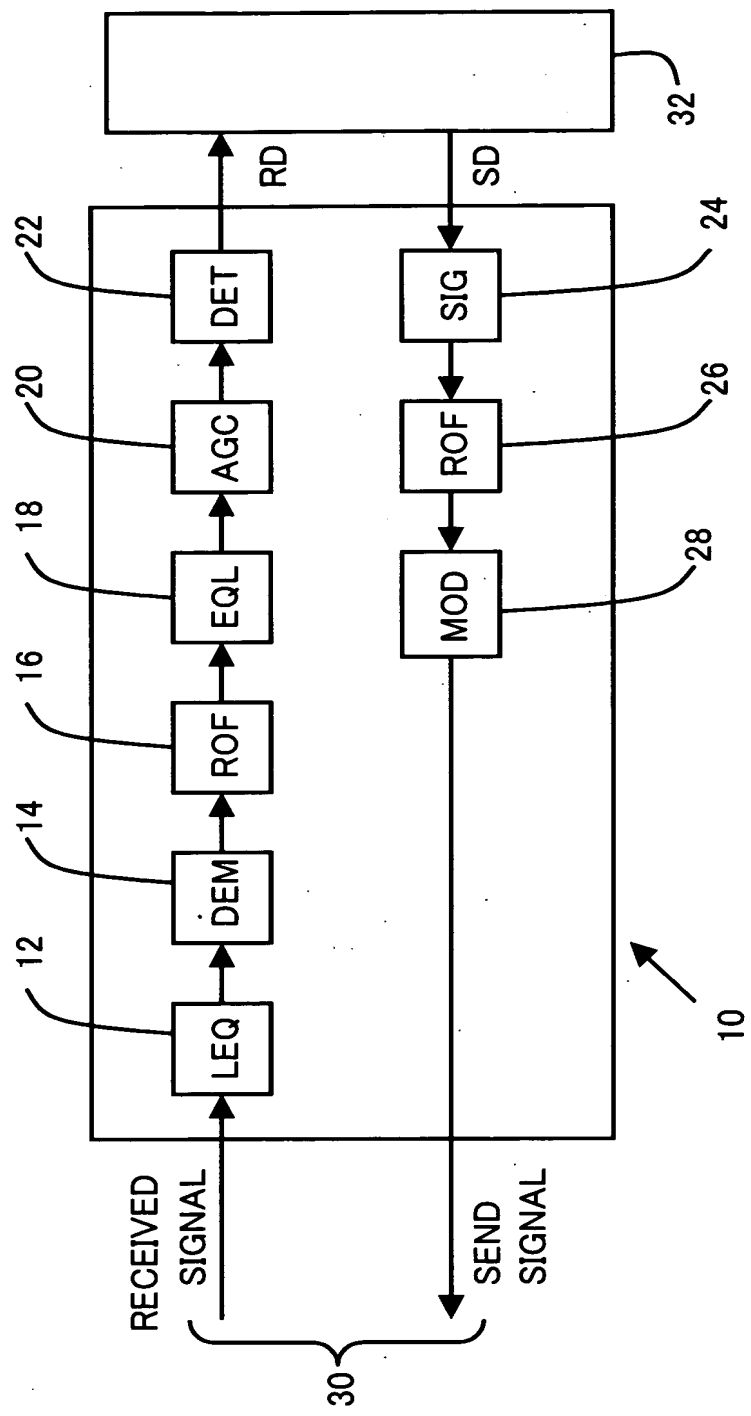
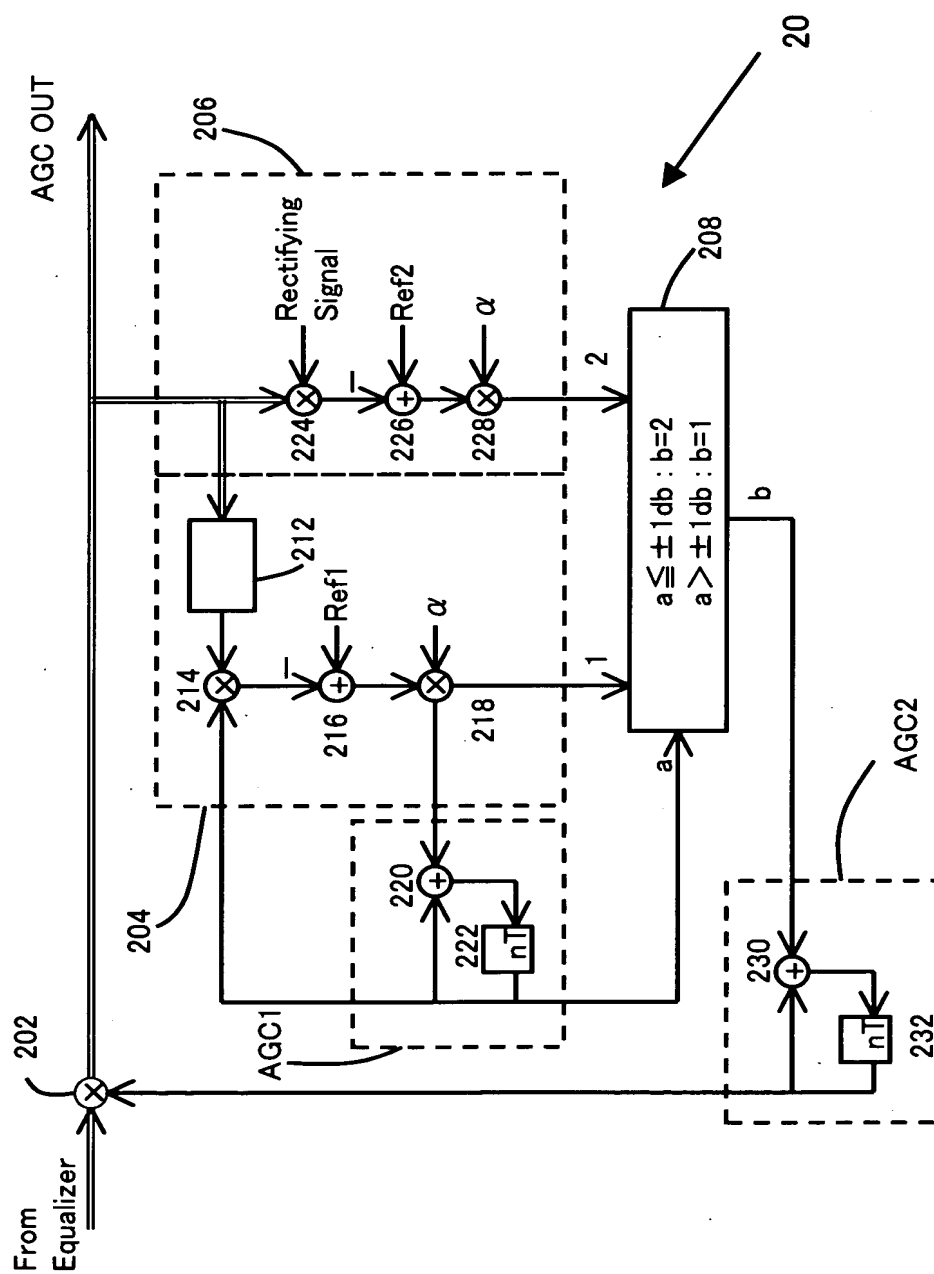


FIG. 1



**FIG. 2**

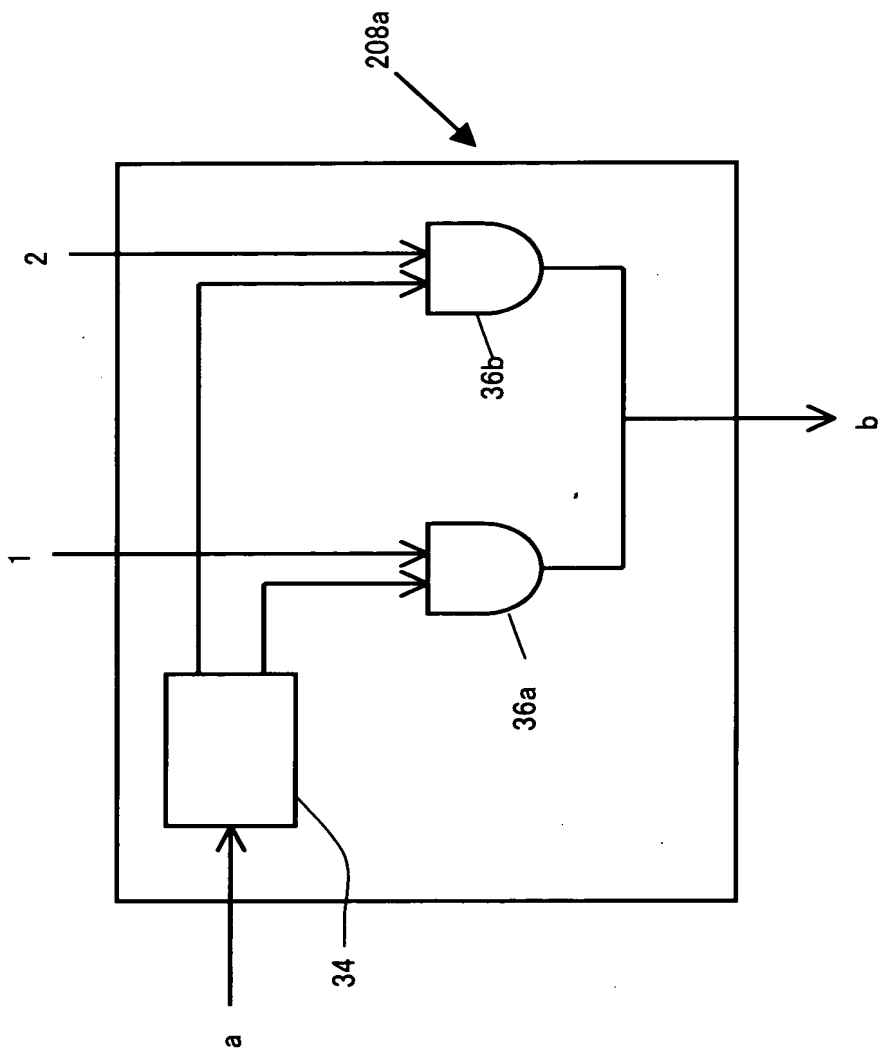


FIG. 3

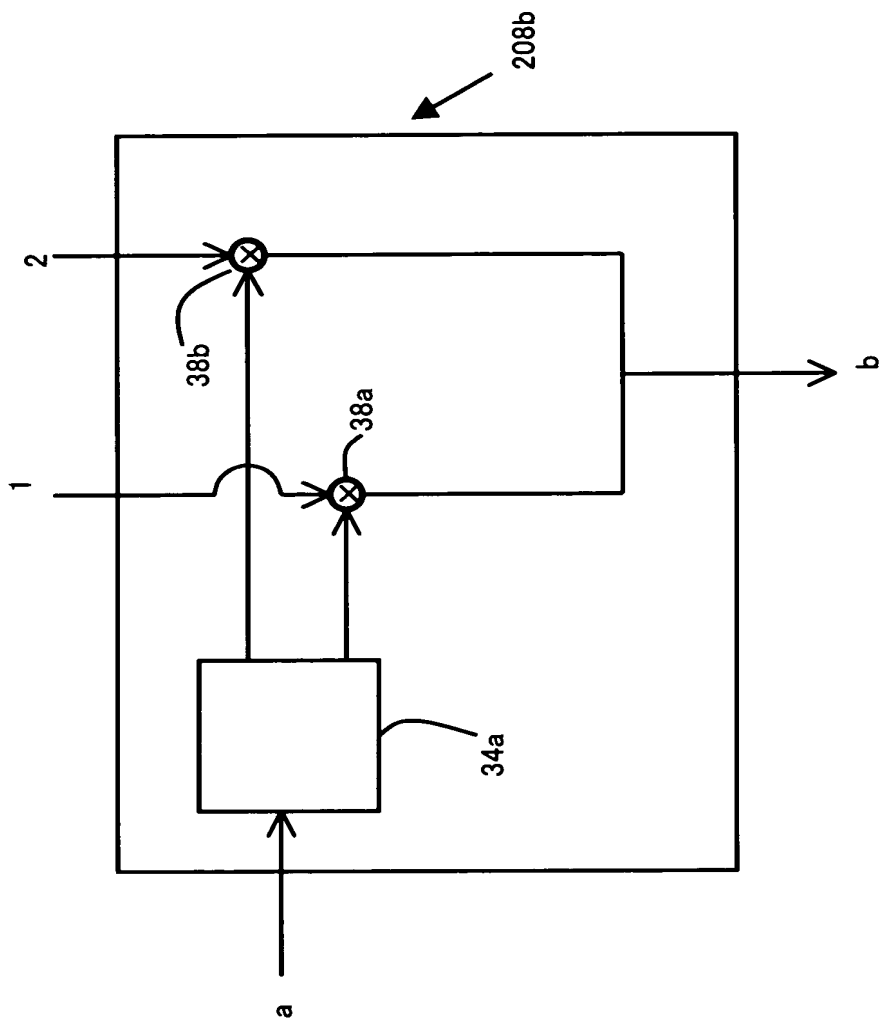


FIG. 4

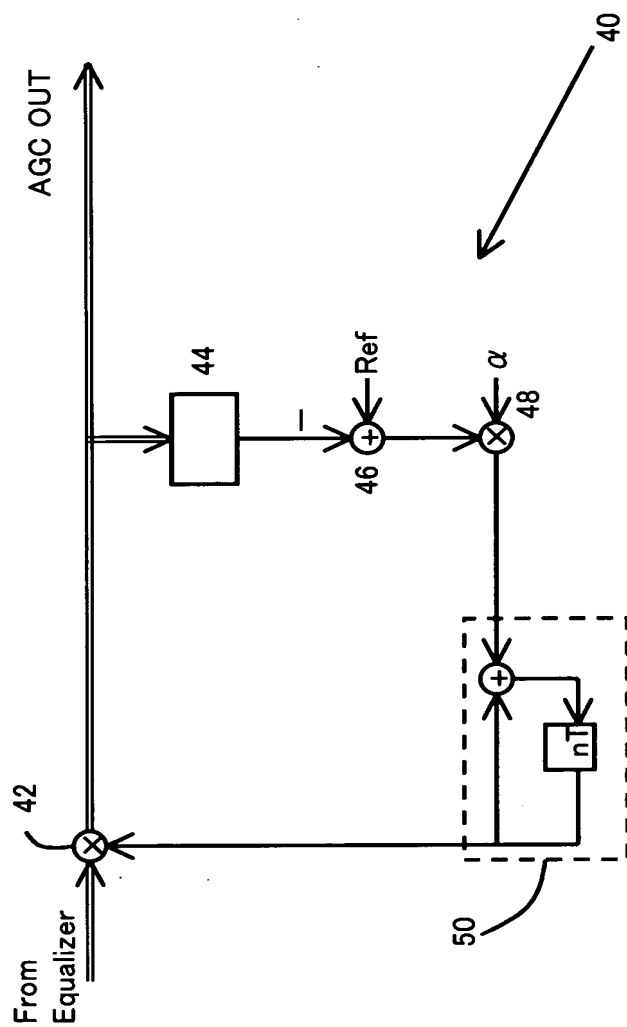


FIG. 5

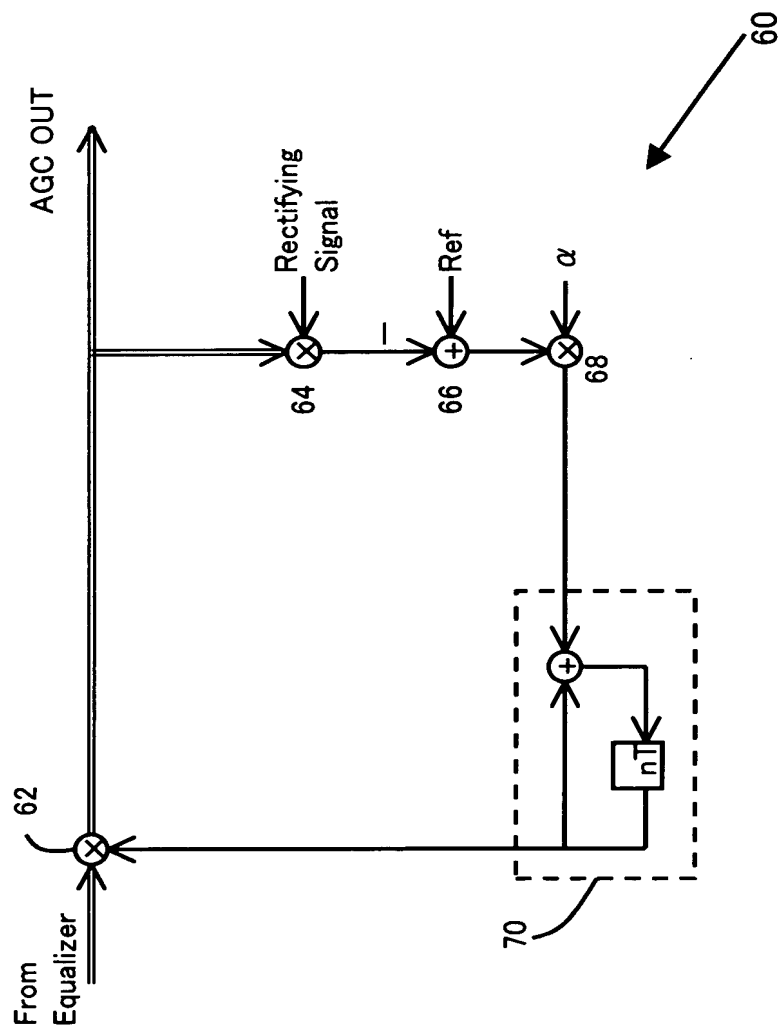


FIG. 6

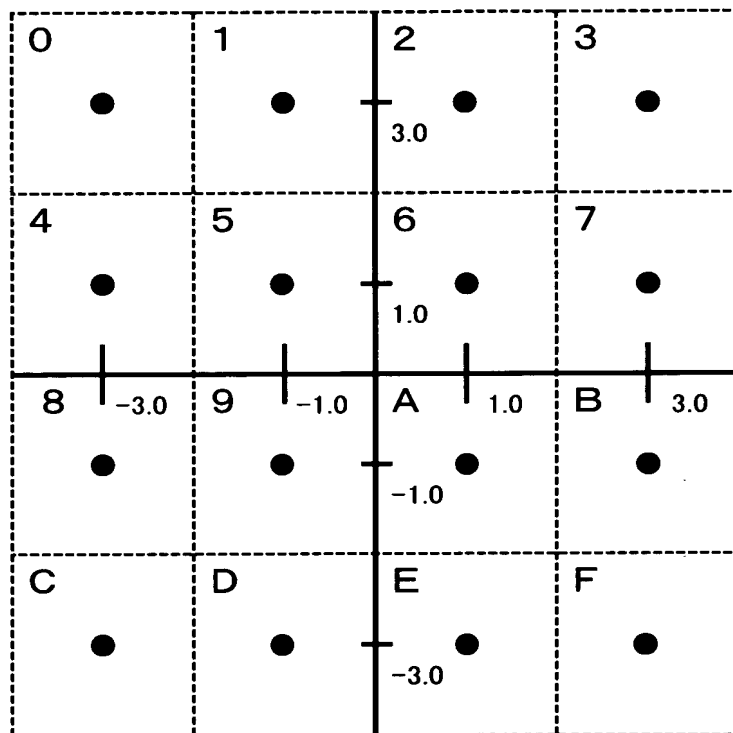
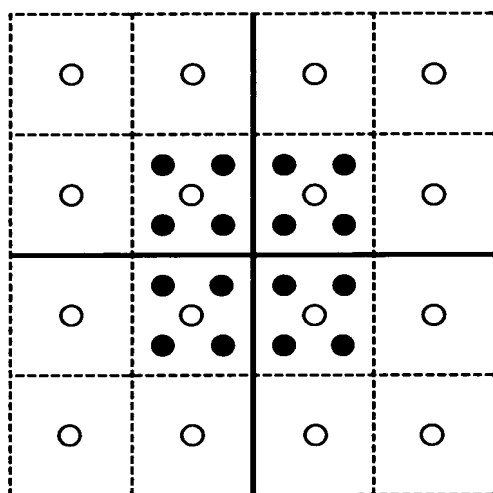


FIG. 7

AREA	DETERMINATION POINT	RECTIFYING SIGNAL	DETERMINATION POINT x RECTIFYING SIGNAL
0	-3.0, 3.0	-0.333, -0.333	2.0, 0.0
1	-1.0, 3.0	-0.2, -0.6	2.0, 0.0
2	1.0, 3.0	0.2, -0.6	2.0, 0.0
3	3.0, 3.0	0.333, -0.333	2.0, 0.0
4	-3.0, 1.0	-0.6, -0.2	2.0, 0.0
5	-1.0, 1.0	-1.0, -1.0	2.0, 0.0
6	1.0, 1.0	1.0, -1.0	2.0, 0.0
7	3.0, 1.0	0.6, -0.2	2.0, 0.0
8	-3.0, -1.0	-0.6, 0.2	2.0, 0.0
9	-1.0, -1.0	-1.0, 1.0	2.0, 0.0
A	1.0, -1.0	1.0, 1.0	2.0, 0.0
B	3.0, -1.0	0.6, 0.2	2.0, 0.0
C	-3.0, -3.0	-0.333, 0.333	2.0, 0.0
D	-1.0, -3.0	-0.2, 0.6	2.0, 0.0
E	1.0, -3.0	0.2, 0.6	2.0, 0.0
F	3.0, -3.0	0.333, 0.333	2.0, 0.0

FIG.8





●:INPUT SIGNAL POINT  
O:IDEAL SIGNAL POINT

FIG. 9